REMARKS

Reconsideration of the instant application is respectfully requested. The present amendment is responsive to the Office Action of January 27, 2005, in which claims 1-6 are presently pending. Of those, claims 1-4 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,072,233 to Corisis, et al. In addition, claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Corsis, et al. However, the Examiner has further indicated that claim 5 would be allowable over the references of record if rewritten in independent form. For the following reasons, it is respectfully submitted that the application is in condition for allowance.

As an initial matter, paragraph [0001] of the electronically filed specification has been amended to include the issued patent number (6,762,489) of the related parent application number, thus addressing the Examiner's objection on page 2 of the present office action. In addition, Figures 1 and 2 have been amended to include a --Prior Art-- legend, as also requested by the Examiner, with replacement sheet being submitted herewith.

Claim 2 has been amended, as indicated above, to incorporate the Examiner's suggested changes, and it is respectfully requested that the Examiner's objection thereto be withdrawn. Claim 4 has also been amended to correct a typographical error discovered therein.

With regard to the rejections based on the art of record, claim 1 has been amended to more particularly point out that the first and second translation layers are further configured so as to fan out the signals from the first grid to the second grid. Support for this claim feature is found at least in paragraph [0017] of the specification, and in Figure 4. This feature, however, is not taught or suggested by Corisis. Rather, Corisis teaches a grid array package "that allows the stacking of one array upon another." (col. 2, lines 36-

38) Moreover, as stated in column 2, lines 61-65, Corisis teaches that "[t]his isolated connection connects to an adjacent ball on a different FBGA stack above or below the particular isolated connection since in ***common pin layouts of the devices stacked together***, each device requires an isolated connection to the PC board." (Emphasis added)

In other words, the conductor patterns are configured not to fan out connections between layers, but to allow stacking of like-configured substrates. As such, Corisis does not teach the claimed jogging structure having first and second translation layers (as set forth above) wherein the translation layers are further configured to fan out the signals. Accordingly, each of the §102 rejections to claims 1-4, and §103 rejections to claim 6 have been overcome, and it is respectfully requested that the same be withdrawn.

Finally, claim 7 has been added to incorporate the same subject matter included in allowable claim 5 (as originally filed), and would therefore constitute allowable subject matter.

For the above stated reasons, it is respectfully submitted that the present application is now in condition for allowance. No new matter has been entered and no additional fees are believed to be required. However, if any fees are due with respect to this Amendment, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,
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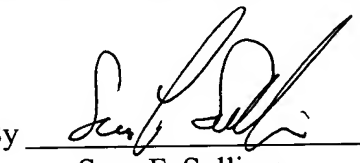
By 
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